



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Assistant Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
AND REVOCATION OF PRIOR POWERS

As assignee of record of the entire interest of the U.S. patent applications identified on the attached Schedule A, all powers of attorney previously given are hereby revoked and the following attorney(s) and/or agent(s) are hereby appointed to prosecute and transact all business connected therewith:

Mark A. Dalla Valle, Reg. No. 34,147
Thomas J. Ring, Reg. No. 29,971
Timothy J. Keefer, Reg. No. 35,567
Annette M. McGarry, Reg. No. 34,671
Gary R. Gillen, Reg. No. 35,157
David A. Frey, Reg. No. 43,618
Douglas S. Rupert, Reg. No. 44,434
Dennis K. Scheer, Reg. No. 39,356

and the following members of the National Semiconductor Corporation Intellectual Property Department: Christopher J. Byrne (32,204); Eugene C. Conser (39,149); John L. Maxin (34,668); Coleman F. Reif (38,593); Allen R. Tremain (40,207); Andrew S. Viger (28,552); and Peter Y. Wang (40,452) as our attorney(s) or agent(s) to prosecute and to transact all business in the U.S. Patent and Trademark Office connected therewith.

Please change the correspondence address for the above-identified application and direct all future correspondence to the following address:

Mark A. Dalla Valle
Wildman, Harrold, Allen & Dixon
225 West Wacker Drive
Chicago, Illinois 60606
Telephone: (312) 201-2000
Facsimile: (312) 201-2555

Dated: 6-27-01

4
JUL 12 2001
RECEIVED
Technology Center 2600
JUL 12 2001
RECEIVED
TC 2800 MAIL ROOM
JC 8/14

National Semiconductor Corporation
By: Christopher J. Byrne
Christopher J. Byrne
Director of Intellectual Property and Technology Licensing

09/14/983 Gp & 664



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
TRANSMITTAL LETTER

REVOCATION OF PRIOR POWERS, APPOINTMENT OF NEW COUNSEL and
CHANGE OF CORRESPONDENCE ADDRESS

Assistant Commissioner for Patents
Washington, D.C. 20231

RECEIVED

JUL 12 2001

Technology Center 2600

Dear Sir:

In connection with the filings of the enclosed referenced U.S. patent applications (see attached Schedule A) submitted herewith are the following materials to be filed in the United States Patent Office.

1. Power of Attorney by Assignee and Revocation of Previous Powers in favor of the undersigned executed by: National Semiconductor Corporation, M/S D3-579, 2900 Semiconductor Drive, Santa Clara, CA 95051.

Also, Applicant respectfully requests all correspondence in respect to this application be directed to Applicant's attorneys as follows:

CORRESPONDENCE ADDRESS

Mark A. Dalla Valle
WILDMAN, HARROLD, ALLEN & DIXON
225 West Wacker Drive
Chicago, Illinois 60606-1229
Telephone: (312) 201-2000
Facsimile: (312) 201-2555

Respectfully submitted,

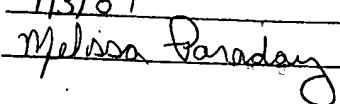


Mark A. Dalla Valle
Reg. No: 34, 147

Enclosures

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on
7/13/01



TC 200 MAIL ROOM
12 2001

RECEIVED



SCHEDULE A

Applicant: National Semiconductor Corporation

RECEIVED
JUL 12 2001
Technology Center 2600

RECEIVED
JUL 12 2001
MAIL ROOM
TC 2600

<u>U.S. Serial No.</u>	<u>U.S. Filing Date</u>	<u>Title</u>	<u>Inventor</u>
09/746,903	12/22/00	Microsequencer Microcode Bank Switched Architecture	David L. Weigand
09/746,680	12/22/00	System, Method, and Apparatus for a Microsequencer Microarchitecture of...	David L. Weigand
09/675,311	09/29/00	Voltage Control Oscillator with Stable Free Run Frequency Using Current Clamping	Hon Kin Chiu et al.
09/746,752	12/22/00	Discontinuous Transmission Architecture	David L. Weigand
09/769,573	1/25/01	Multiple-Band Wireless Transceiver with Quadrature Conversion Transmitter and...	Hak Ming Pau
09/769,877	1/25/01	Multiple-Band Wireless Transceiver with Quadrature Conversion Transmitter and...	Hak Ming Pau
09/746,902	12/22/00	Microwire Paging Architecture	David Weigand
09/746,909	12/22/00	Microwire Bank Switched Architecture	David Weigand
09/847,129	5/1/01	Oscillator Control Circuitry for Phase Lock Loop Providing Enhanced Phase Noise...	Kim Yeow Wong et al.
09/779,150	2/8/01	Microprocessor with Hardware Controlled Power Management	Robert Maher et al.
09/746,643	12/22/00	System, Method, and Apparatus for Low Power Dual Clock Microsequencer...	David Weigand
09/379,277	8/23/99	CMOS Digital Inverter Circuit with Balanced Signal Edge Delays	Steven Mark Macaluso
09/383,162	8/25/99	Voltage Sample and Hold Circuit for Low Leakage Charge Pump	Steve Lo et al.
60/153,013	9/9/99	Multiplexed Video Signal Interface Signal, System and Method	Andrew Morrish et al.
09/602,175	6/22/00	Multiplexed Video Signal Interface Signal, System and Method	Andrew Morrish et al.
09/698,739	10/27/00	Multiplexed Video Signal Interface Signal, System and Method	Peyman Hojabri
09/429,411	10/28/99	Analog Amplifier with Monotonic Transfer Function	Peyman Hojabri et al.



7558,927	4/26/00	Frequency Synthesizer with Digital Frequency Lock Loop	Christian Olgaard et al.
09/772,033	1/29/01	Amplifier with Controllable Variable Signal Gain	David Edward Bien
09/753,179	1/2/01	Method and Circuit for Improving Lock-Time Performance for a Phase-Locked Loop	David Lindsay Broughton et al.
09/675,987	9/29/00	Saturation Compensating Analog to Digital Converter	Christian Olgaard et al.
09/668,963	9/25/00	Differential Conversion Circuit	Mark Alan Jones
09/643,275	8/22/00	GSM Transceiver with Time Division Duplexed Operations for Receiving Date...	Christian Olgaard et al.
09/599,620	6/22/00	Voltage Clamping Circuit	Ronald William Page
09/429,144	10/28/99	High Gain, Current Driven, High Frequency Amplifier	Andrew Morrish et al.
09/053,193	4/1/98	Transient Signal Detector	Duncan James Bremner
09/294,755	4/19/99	Switched Capacitor Filter Circuit Having Reduced Offsets and Allowing...	Laurence Douglas Lewicki
60/172,546	12/17/99	Telephone Receiver Circuit with Sidetone Signal Generator Controlled...	David Lind Weigand
09/482,380	1/13/00	Circuit for Removing In-Band FSK Signals Without Muting of Receiver	Theo Ary Asmund Tielens et al.
09/481,334	1/12/00	Extended Power Ramp Table for Power Amplifier Control Loop	Christian Olgaard
09/481,925	1/12/00	Telephone Receiver Circuit with Dynamic Sidetone Signal Generator Controlled...	David Lind Weigand
60/067,764	12/10/97	Data Signal Baseline Error Detector	Wong Hee et al.
09/076,183	5/12/98	Control Loop for Data Signal Baseline Correction	Wong Hee et al.
09/076,261	5/12/98	Data Signal Baseline Error Detector	Wong Hee et al.
09/076,260	5/12/98	Control Loop for Adaptive Equalization of a Data Signal	Wong Hee et al.
60/069,030	12/10/97	Control Loop for Data Signal Baseline Correction	Wong Hee et al.
09/076,256	5/12/98	Control Loop for Adaptive Multilevel Detection of a Data Signal	Wong Hee et al.



60/069,091	12/10/97	Digital Signal Processing Control Circuit for Controlling Corrections of Input...	Wong Hee et al.
60/069,031	12/10/97	Digital Interface Circuit	Wong Hee et al.
60/069,028	12/10/97	Control Loop for Adaptive Equalization of a Data Signal	Wong Hee et al.
09/076,187	5/12/98	Distributive Encoder for Encoding Error Signals which Represent Signal Peak Errors...	Wong Hee et al.
09/368,321	8/3/99	Low Voltage Circuit for Generating Current with a Negative Temperature Coefficient	Gregory J. Smith et al.
09/323,308	6/1/99	Low Noise Buffer Circuit for Increasing Digital Signal Transition Slew Rates	David R. MacQuigg
09/322,681	5/28/99	Digitally Controlled Signal Magnitude Control Circuit	Peyman Hojabri et al.
09/286,363	4/5/99	Low Voltage Class AB Amplifier with Gain Boosting	Rudy G.H. Eschauzier et al.
09/348,533	7/7/99	Digitally Controlled Signal Magnitude Control Circuit	Peyman Hojabri et al.
09/176,633	10/22/98	Distributive Encoder for Encoding Error Signals Which Represent Signal...	Wong Hee et al.
60/069,029	12/10/97	Control Loop for Multilevel Sampling of a Data Signal	Wong Hee et al.
09/127,221	7/31/98	Low Noise Electrostatic Discharge Protection Circuit for Mixed Signal CMOS Integrated...	Dan Ion Hariton et al.
09/294,289	4/19/99	Switched Capacitor Filter Circuit having Reduced Offsets and Providing...	Laurence Douglas Lewicki
09/294,635	4/19/99	Switched-Capacitor Cosine Filter Circuit	Laurence Douglas Lewicki
09/294,696	4/19/99	Chopper-Stabilized Telescopic Differential Amplifier	Laurence Douglas Lewicki
09/746,631	12/22/00	System, Method, and Apparatus for Low Power Operation Mode for...	David L. Weigand
09/076,186	5/12/98	Peak Error Detector	Hee Wong et al.
09/076,263	5/12/98	Digital Interface Circuit	Hee Wong et al.
9/053,110	4/1/98	Signal Line Driving Circuit with Self-Controlled Power Dissipation	Duncan James Bremner



09/599,380	6/22/00	Voltage Comparator Circuit with Hysteresis	Ronald William Page
09/368,104	8/3/99	Bandgap-Based Reference Voltage Generator Circuit with Reduced Temperature...	Gregory J. Smith et al.
09/413,925	10/7/99	Complementary CMOS Differential Amplifier Circuit	Peyman Hojabri
08/791,382	11/17/98	Multiple Stage Adaptive Equalizer	Hee Wong et al.
60/069,027	12/10/97	Peak Error Detector	Hee Wong et al.
60/069,044	12/10/97	Signal Gating Controller for Enhancing Convergency of MLT3 Data Receivers	Hee Wong et al.
09/370,797	11/19/98	Multiple Stage Adaptive Equalizer	Hee Wong et al.
08/791,382	1/30/97	Multiple Stage Adaptive Equalizer	Hee Wong et al.
90/005,847	10/17/00	Multiple Stage Adaptive Equalizer	Hee Wong et al.
09/176,783	10/22/98	Variable Gain Current Summing Circuit with Mutually Independent Gain and Biasing	Abhijit Phanse et al.
09/076,425	5/12/98	Signal Gating Controller for Enhancing Convergency of MLT3 Data Receivers	Wong Hee et al.
09/651,950	8/31/00	System, Method and Apparatus for Creating Character Boxes for on Screen Displays	Andrew Morrish
09/651,953	8/31/00	Enhanced Color Palette for On-Screen Displays	Andrew Morrish
09/556,607	4/21/00	Apparatus and Method for Converting Analog Signal to Pulse-Width-Modulated Signal	Arthur Joseph Kalb
09/559,202	6/22/00	Vertical Blanking Circuit and Bias Clamp Boost Supply	Andy Morrish
09/263,134	3/5/99	Switched Capacitor Bias Circuit for Generating a Reference Signal Proportional...	Laurence Douglas Lewicki et al.
09/138,722	8/24/98	Tone Pulse Signal Generator with Automatic Gain Control for Subscriber Line Interface...	Duncan James Bremner et al.
09/438,021	11/10/99	Transient Signal Detector	Duncan James Bremner
09/243,641	2/3/99	Low Power Class A Amplifier Circuit	Kwok Fu Chiu
09/262,391	3/4/99	Power Supply Regulator Circuit for Voltage-Controlled Oscillator	James R. Kuo
09/298,412	4/23/99	Liquid Crystal on Silicon (LCOS) Display Pixel with Multiple Storage Capacitors	Philip John Cacharelis



60/146,098	7/21/99	Apparatus and Method for Establishing a Data Communication Interface to Control...	Gregory J. Smith et al.
09/614,081	7/11/00	Apparatus and Method for Establishing a Data Communication Interface to Control...	Gregory J. Smith et al.
09/102,159	6/22/98	Overshoot Control and Damping Circuit for High Speed Drivers	Peyman Hojabri
09/658,704	9/8/00	Microsequencer for Dynamic Packetized Data Processing	David L. Weigand
09/666,761	9/21/00	Packetized Data Signal Processor with Dynamically Configurable Distributed...	David Lind Weigand
09/746,904	12/22/00	Microsequencer Halt Instruction	David L. Weigand
09/746,681	12/22/00	Multibyte Microwire Engine	David L. Weigand
09/751,152	12/27/00	Microwire Dynamic Sequencer Pipeline Stall	David L. Weigand
08/968,675	11/12/97	Complementary Class AB Current Mirror Circuit	James Bales
09/176,784	10/22/98	Gain Control Signal Generator that Tracks Operating Variations Due to Variations...	Abhijit Phanse et al.
09/366,237	8/3/99	Precision Voltage Reference Circuit with Temperature Compensation	Gregory J. Smith et al.
09/312,182	5/14/99	Character Line Address Counter Clock Signal Generator for on Screen Displays	Andrew Morrish et al.
09/290,028	4/9/99	Self-Biased, Phantom-Powered and Feedback-Stabilized Amplifier for Electret Microphone	Rudy G.H. Eschauzier et al.
09/505,028	2/16/00	Apparatus and Method for a Fast Locking Phase Locked Loop	Christian Olgaard